Amendments to the Claims

Please cancel claim 29.

Please amend claims 31, 32, 34, 37, 39 and 40 as shown below.

Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-20 (Cancelled).

21. (Previously presented) A semiconductor circuit arrangement on a substrate comprising:

a doped semiconductor layer having a first conductivity type disposed on the substrate;

an insulating layer disposed on the doped semiconductor layer;

a charge storing layer configured for storing an electrical charge disposed on the insulating layer;

at least one deep trench that penetrates through the charge storing layer and extends into the doped semiconductor layer; and

a shallow trench arranged in the doped semiconductor layer, wherein the shallow trench does not penetrate through the charge storing layer and the insulating layer and the shallow trench extends about laterally symmetrical in all directions beyond an edge of the deep trench.

22. (Previously presented) The semiconductor circuit arrangement of claim 21, where the charge storing layer is a conducting layer.

23. (Previously presented) The semiconductor circuit arrangement of claim 21, where the charge storing layer is an insulating layer.

24. (Previously presented) The semiconductor circuit arrangement of claim 21, where the at least one deep trench penetrates through the doped semiconductor layer into the substrate.

25. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a second doped semiconductor layer having a second conductivity type disposed between the substrate and the doped semiconductor layer, where the second conductivity type is opposite to the conductivity type of the doped semiconductor layer.

26. (Previously presented) The semiconductor circuit arrangement of claim 25, further comprising the at least one deep trench penetrating through the doped semiconductor layer and extending into the second doped layer.

27. (Previously presented) The semiconductor circuit arrangement of claim 25, further comprising the at least one deep trench penetrating through the doped semiconductor layer and the second semiconductor layer into the substrate.

28. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a conductive layer and a second insulating layer where the second insulating layer is disposed on the charge storing layer and the conductive layer is disposed on the second insulating layer.

29-30. (Cancelled)

31. (Currently amended) The semiconductor circuit arrangement of claim 21 [[30]], where the shallow trench extends laterally about 50 nm beyond the edge of the deep trench.

32. (Currently amended) The semiconductor circuit arrangement of claim 21 [[29]], where the shallow trench contains an insulating material.

33. (Previously presented) The semiconductor circuit arrangement of claim 32, where the insulating material is polycrystalline silicon.

34. (Currently amended) The semiconductor circuit arrangement of claim 21 [[29]], ~~further comprising at least one shallow trench through which~~ wherein no deep trench penetrates said shallow trench.

35. (Previously presented) The semiconductor circuit arrangement of claim 34, where the semiconductor arrangement forms a logic circuit arrangement.

36. (Cancelled).

37. (Currently amended) The semiconductor circuit arrangement of claim 21 [[29]], ~~further comprising a shallow trench~~ where the deep trench penetrates through the bottom of ~~the~~ said shallow trench.

38. (Previously presented) The semiconductor circuit arrangement of claim 37, where the semiconductor arrangement is a memory circuit arrangement.

39. (Currently amended) The semiconductor circuit arrangement of claim 21 [[29]], where the charge storing layer extends at least partly over the shallow trench.

40. (Currently amended) The semiconductor circuit arrangement of claim 21 [[29]], where the second electrically insulating layer extends at least partly over the shallow trench.

41. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a second charge storing layer disposed on the charge storing layer and the deep trench does not penetrate into the second charge storing layer.

42. (Previously presented) The semiconductor circuit arrangement of claim 41, further comprising an opening in the second charge storing layer above the deep trench.

43. (Previously presented) The semiconductor circuit arrangement of claim 42, where the edges of the opening are a smaller distance apart than the lateral edges of the deep trench.

44. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising an insulating material that fills the deep trench.

45. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising an insulating material disposed on the wall of the at least one deep trench.

46. (Previously presented) The semiconductor circuit arrangement of claim 45, wherein the electrically insulating material on the wall of the at least one deep trench is silicon dioxide.

47. (Previously presented) The semiconductor circuit arrangement of claim 45, where the at least one deep trench is filled with an electrically conductive or semi-conductive material and the material is isolated from the trench wall with the electrically insulating material.

48. (Previously presented) The semiconductor circuit arrangement of claim 47, wherein the conductive or semi-conductive material is polysilicon.

49-72 (Cancelled).